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Application Number	10766761
Filing Date	2004-01-28
First Named Inventor	Craig E. Hampel
Art Unit	2611
Examiner Name	Jia Lu
Attorney Docket Number	RBUS 1309-1

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/TW/	1	20020054648	A1	2002-05-09	Krummrich et al.	

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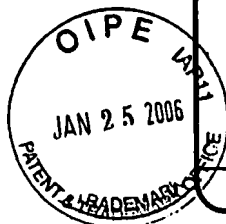
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Substitute for form 1449A/PTO			<b>Complete If Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>			<b>Application Number</b>	10/766,761
(use as many sheets as necessary)			<b>Filing Date</b>	28 January 2004
Sheet <span style="border: 1px solid black; padding: 0 10px;">1</span> of <span style="border: 1px solid black; padding: 0 10px;">2</span>			<b>First Named Inventor</b>	Craig E. Hampel
			<b>Group Art Unit</b>	2637
			<b>Examiner Name</b>	Jayanti K. Patel
			<b>Attorney Docket Number</b>	RBUS 1309-1

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				Filing Date	28 January 2004
				First Named Inventor	Craig E. Hampel
				Group Art Unit	2637
				Examiner Name	Jayanti K. Patel
Sheet	2	of	2	Attorney Docket Number	RBUS 1309-1

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/TW/	C1	EIA/JEDEC Standard No. 8-B (JESD8-B) "Interface Standard for Nominal 3 V/3.3 V Supply Digital Integrated Circuits," (Sept. 1999) 12 pages.	
/TW/	C2	EIA/JEDEC Standard No. 8-6 (EIA/JESD8-6) "High Speed Transceiver Logic (HSTL) A 1.5 V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits," (Aug. 1995) 16 pages.	
/TW/	C3	JEDEC Standard - JESD8-16 "Bus Interconnect Logic (BIC) for 1.2 Volts," (Apr. 2004) 16 pages.	
/TW/	C4	LEE, Ming-Ju Edward et al., "TP 15.3: A 90mW 4Gb/s Equalized I/O Circuit with Input Offset Cancellation" IEEE International Solid-State Circuits Conference, pages 252-253.	

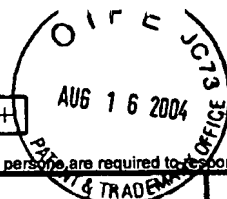
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### Complete if Known

Application Number	10/766,761
Filing Date	28 January 2004
First Named Inventor	Craig E. Hampel
Group Art Unit	2631
Examiner Name	
Attorney Docket Number	RBUS 1309-1

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		Number	Kind Code <sup>2</sup> (if known)			
/TW	A50	5,548,146		Kuroda et al.	08-20-1996	
/TW	A51	6,377,640		Trans	04-23-2002	
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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				Application Number	10/766,761
				Filing Date	28 January 2004
				First Named Inventor	Craig E. Hampel
				Group Art Unit	2631
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/TW/	C27	WIDMER, A.X., et al., "A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code," IBM J. Res. Develop., Vol. 27, No. 5, September 1983, 440-451.		
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## INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Application Number	107/66,761
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First Named Inventor	Craig E. Hampel
Group Art Unit	2631
Examiner Name	Unassigned
Attorney Docket Number	RBUS 1309-1

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	<b>Application Number</b>	10/766,761		
	<b>Filing Date</b>	28 January 2004		
	<b>First Named Inventor</b>	Craig E. Hampel		
	<b>Group Art Unit</b>	2631		
	<b>Examiner Name</b>	Unassigned		
<b>Sheet</b>	3	<b>of</b>		
	<b>Attorney Docket Number</b>	RBUS 1309-1		

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS				
Examiner Initials <sup>*</sup>	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T <sup>2</sup>
/TW/	C1	U.S. Patent Application No. 10/278,708 filed 22 October 2002, entitled "Phase Adjustment Apparatus and Method for a Memory Device Signaling System."		
/TW/	C2	DANIELE, N. et al., "Principle and Motivations of UWB Technology for High Data Rate WPAN Applications," SOC 2003, 4 pages.		
/TW/	C3	WIN, MOE Z., et al., "Impulse Radio: How it Works," IEEE Communications Letters 2(2), Feb. 1998, 36-38.		
/TW/	C4	DANIELE, NORBERT, "Ultra Wide Band Principles and Applications for Wireless Communications," CEA-LETI Annual Review, 25 and 26 June 2002, 24 pages.		
/TW/	C5	U.S. Patent Application No. 09/941,079 filed 28 August 2001 entitled "Clock Data Recovery with Selectable Phase Control Input."		
/TW/	C6	Yang, Chih-Kong Ken "Design of High-Speed Serial Links in CMOS" Technical Report No. CSL-TR-98-775, Sponsored By Center for Integrated Systems, Sun Microsystems and LSI Logic Inc. December 1998, pp. 1-182.		
/TW/	C7	RaSer™ X Product Brief, "Highly Flexible 10 Gbps Backplane Serial Link Interface," Copyright 2003 Rambus, Inc., all rights reserved, 2 pages.		
/TW/	C8	Yellowstone Technology Brief, "High Performance Memory Interface Technology," Copyright 2003 Rambus, Inc., all rights reserved, 2 pages.		
	C9			
	C10			
	C11			

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Application Number	10/766,761
Filing Date	28 January 2004
First Named Inventor	Craig E. Hampel
Art Unit	Unassigned
Examiner Name	Unassigned
Attorney Docket Number	RBUS 1309-1

## U. S. PATENT DOCUMENTS

## FOREIGN PATENT DOCUMENTS

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of

2

Application Number

10/766,761

Filing Date

28 January 2004

First Named Inventor

Craig E. Hampel

Art Unit

Unassigned

Examiner Name

Unassigned

Attorney Docket Number

RBUS 1309-1

**NON PATENT LITERATURE DOCUMENTS**

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/TWI/	C1	U.S. Patent Application No. 10/278,478, Filed 22 October 2002 entitled "Timing Calibration Apparatus and Method for a Memory Device Signaling System"	
/TWI/	C2	Chang, Kun-Yung "Design of a CMOS Asymmetric Serial Link" A Dissertation Submitted to the Department of Electrical Engineering and the Committee on Graduate Studies of Stanford University August 1999, 119 pages	

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			Filing Date		
			First Named Inventor		
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		Number	Kind Code <sup>2</sup> (if known)			
/TW/	A1	4,384,354		Crawford et al.	05/17/1983	
/TW/	A2	5,122,978		Merrill	06/16/1992	
/TW/	A3	5,436,908		Fluker et al.	07/25/1995	
/TW/	A4	5,859,881		Ferraiolo et al.	01/12/1999	
/TW/	A5	6,047,346		Lau et al.	04/04/2000	
/TW/	A6	6,219,384		Kliza et al.	04/17/2001	
/TW/	A7	6,282,210		Rapport et al.	08/28/2001	
/TW/	A8	6,359,931		Perino et al.	03/19/2002	
/TW/	A9	6,396,329		Zerbe	05/28/2002	
/TW/	A10	6,442,644		Gustavson et al.	08/27/2002	
/TW/	A11	6,448,815		Talbot et al.	09/10/2002	
/TW/	A12	6,463,392		Nygaard et al.	10/08/2002	
/TW/	A13	6,469,555		Lau et al.	10/22/2002	
/TW/	A14	6,473,439		Zerbe et al.	10/29/2002	
/TW/	A15	6,510,503		Gillingham et al.	01/21/2003	
/TW/	A16	6,539,072		Donnelly et al.	03/25/2003	
/TW/	A17	6,556,934		Higashide	04/29/2003	
/TW/	A18	6,643,787		Zerbe et al.	11/04/2003	
/TW/	A19	2003/0026399		Carlson	02/06/2003	

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		Office <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>5</sup> (if known)				
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				Application Number	
				Filing Date	28 January 2004 (Herewith)
				First Named Inventor	Craig E. Hampel
				Group Art Unit	
				Examiner Name	
Sheet	2	of	4	Attorney Docket Number	RBUS 1309-1

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Sheet	3	of	4	RBUS 1309-1	

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/TW/	C1	PARIS, LLUIS ET AL, "WP 24.3 A 800MB/s 72Mb SDRAM with Digitally-Calibrated DLL," IEEE International Solid-State Circuits Conference (1999), 13 pages.	
/TW/	C2	NAKASE, YASUNOBU ET AL, "Source-Synchronization and Timing Vernier Techniques for 1.2-GB/s SDRAM Interface," IEEE Journal of Solid-State Circuits, Vol. 34, No. 4 (Apr. 1999), 494-501.	
/TW/	C3	GILLINGHAM, PETER, "SLDRAM Architectural and Functional Overview," SDRAM Consortium (29 Aug 1997), 1-14.	
/TW/	C4	"Draft Standard for a High-Speed Memory Interface (SyncLink)", Draft 0.99 IEEE P1596.7-199X (1996), 56 pages	
/TW/	C5	GILLINGHAM, PETER, "SLDRAM: High-Performance, Open-Standard Memory," IEEE (1997), 29-39	
/TW/	C6	SLDRAM Inc., "400 Mb/s/pin SDRAM," Draft Advance (9 Jul 1998), 1-69.	
/TW/	C7	ZERBE, JARED ET AL., U.S. Patent Application No. 09/776,550 filed 2 February 2001, entitled "Method and Apparatus for Evaluating and Calibrating a Signaling System."	
/TW/	C8	ZERBE, JARED ET AL, U.S. Patent Application No. 09/976,170 filed 21 October 2001, entitled "Method and Apparatus for Evaluating and Optimizing a Signaling System."	
/TW/	C9	RAMBUS "Direct Rambus Short Channel Layout Guide, Version 0.95" (August 2001), 40 pages	
/TW/	C10	RAMBUS "Direct Rambus Long Channel Design Guide" (2000), 45 pages	
/TW/	C11	RAMBUS, INC. "RDRAM Direct Rambus Clock Generator" (April 2002), 22 pages	

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/TW/	C13	REDWOOD TECHNOLOGY BRIEF "High Performance Parallel Bus Interface Technology", Copyright 2003 Rambus, Inc., all rights reserved, 2 pages.	
/TW/	C14	LEWIS, DAVE, "Easy-to-Use LVDS Serdes for the Serdes Neophyte" National Semiconductor, (16 June 2003), pp. 1-5.	
/TW/	C15	INTEL "How to Measure RDRAM* System Clock Jitter" Application Note AP-667 (June 1999), pp. 1-15	

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